WHAT IS CLAIMED IS:

1. A system capable of automatically reading-out a multiple value of clock frequency from system bus, comprising:

a central processing unit having a storage unit therein, wherein said storage unit holds a multiple value of clock frequency, and wherein said central processing unit is capable of synchronizing with an external device according to a serial initialization packet (SIP) protocol; and

a chipset, wherein said chipset is capable of repeatedly selecting a multiple value of clock frequency to serve as a parameter in a serial initialization packet protocol until a synchronizing multiple clock frequency is found.

2. The system of claim 1, wherein said system further including a counter is capable of generating a new counting value after each failed attempting to synchronize.

3. The system of claim 2, wherein said multiple value of clock frequency is changed by according to said counting value.

4. The system of claim 1, wherein said multiple value of clock frequency is selected and said serial initialization packet protocol is executed again, when said chipset cannot be synchronizing with said central processing unit, otherwise, said multiple value of clock frequency is retrieved from said central processing unit and compared with said selected multiple value of clock frequency, and if said two values are different, said preset multiple value of clock frequency is replaced by said value sent from said central processing unit.

5. The system of claim 4, wherein said central processing unit is reset before said serial initialization packet protocol is executed again.

6. The system of claim 4, wherein said system further including a counter is capable of generating a new counting value after each failed attempt to synchronize.

7. The system of claim 6, wherein said multiple value of clock frequency is changed by according to said counting value.

8. A method of automatically reading-out a multiple value of clock frequency between a central processing unit and a system bus, wherein said central processing unit provides said multiple value of clock frequency, comprising said steps of:

selecting a multiple value of clock frequency;

using said preset multiple value of clock frequency as a parameter in serial initialization packet protocol; and

executing said serial initialization packet protocol and attempting to synchronize with said central processing unit by varying said preset multiple value of clock frequency.

9. The method of claim 8, wherein said method further includes generating a new counting value after each failed attempting to synchronize.

10. The method of claim 9, wherein said multiple value of clock frequency is changed by according to said counting value.

11. The method of claim 8, wherein said step of varying said preset multiple value of clock frequency includes said sub-steps of:

changing said preset multiple value of clock frequency when synchronization fails, using said modified multiple value of clock frequency to serve as a parameter in a serial initialization packet protocol, re-executing said protocol and repeating this step until synchronization is obtained;

retrieving said multiple value of clock frequency from said central processing unit when synchronization is successful; and

comparing said retrieved multiple value of clock frequency with said preset multiple value of clock frequency, if said two values are different, said preset multiple value of clock frequency is replaced by said retrieved value.

12. The method of claim 11, wherein said central processing unit is reset before said serial initialization packet protocol is executed again.

13. The method of claim 11, wherein said method further includes generating a new counting value after each failed attempting to synchronize.

14. The method of claim 13, wherein said multiple clock frequency value is changed by according to said counting value.